

JSS Focus Issue on Gallium Oxide Based Materials and Devices

Implementation of a 900 V Switching Circuit for High Breakdown Voltage β-Ga₂O₃ Schottky Diodes

Yen-Ting Chen,¹ Jiancheng Yang,² Fan Ren, □² Chin-Wei Chang,³ Jenshan Lin, □³ S. J. Pearton, □⁴,* Marko J. Tadjer, □⁵ Akito Kuramata,⁶ and Yu-Te Liao □¹,z

This paper presents a switching circuit for high breakdown-voltage Ga_2O_3 vertical Schottky rectifiers. Field-plated edge-terminated (FPET) vertical Schottky diodes were fabricated on a 20- μ m thick Si-doped n-type Ga_2O_3 drift layer which was grown on the 650- μ m thick β - Ga_2O_3 substrate via halide vapor phase epitaxy (HVPE). The measured reverse recovery time of the proposed Ga_2O_3 Schottky diode was 81 ns when switched to a reverse bias voltage of -900 V. The implementation of a switching circuit with the novel Ga_2O_3 diode is the first demonstrated at such a high switching voltage. This paper also provides insights for the practical implementation of the Ga_2O_3 vertical Schottky rectifiers from device fabrication to circuit design.

© The Author(s) 2019. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, http://creativecommons.org/licenses/by/4.0/), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0421907jss]

Manuscript submitted April 12, 2019; revised manuscript received May 8, 2019. Published May 22, 2019. *This paper is part of the JSS Focus Issue on Gallium Oxide Based Materials and Devices*.

With the increasing demands of switching power electronics, widebandgap materials such as silicon carbide (SiC), gallium nitride (GaN), and gallium oxide (Ga₂O₃) have attracted intensive research and development. Wide-bandgap materials can provide higher switching speeds, larger blocking voltages, lower on-resistance (losses), and higher operating temperature ranges than conventional silicon-based materials. Among various wide-bandgap materials, Ga₂O₃ has been considered a potential candidate for next-generation power electronics because of its ultra-wide bandgaps (E_g) of 5.3 eV (α -phase) and 4.9 eV $(\beta\text{-phase}),^{1\text{--}3}$ which translate to around 5–9 MV/cm of a critical electric field. Compared with SiC and GaN, the larger bandgap and melt growth options with Ga₂O₃ offers the potential for higher breakdown fields, high Baliga's Figure of Merit (BFoM), and potentially lower costs in materials and fabrication processes. 1-17 From both theoretical analysis and state-of-the-art prototype, Ga₂O₃ materials help to minimize the size of power devices while maintaining high operation efficiency in switching power electronics.

Since p-type doping, which would improve the breakdown voltage of devices with guard rings, has not yet been demonstrated for Ga₂O₃, the focus has been on field-plated vertical rectifiers to achieve high reverse blocking capability characteristics at high current density. A Schottky rectifier is an attractive unipolar high-power device, which is formed by Schottky non-linear contact on top of a drift region; ^{17–19} it provides fast, soft switching characteristics to avoid unwanted electromagnetic interference (EMI) output.

Switching power devices have been implanted into different applications such as electric motor drivers, DC-DC, and AC/DC converters. $^{18.20,21}$ A common approach is to use hybrid power converters consisting of Si MOSFETs and SiC rectifiers, 22 Schottky rectifiers can provide high-power efficiency due to their fast switching speed, low switching power losses, and high-temperature operation capabilities. 18 Moreover, vertical geometry Ga_2O_3 rectifiers have shown promise for future high-power devices and high-current switching capabilities. Yang et al. 23 demonstrated that Ga_2O_3 vertical rectifiers could reach $2300\,\mathrm{V}$ of breakdown by using a thicker drift layer and lower carrier concentration with field plate design. Also, Ga_2O_3 diodes for high-current switching applications have been demonstrated. $^{24-26}$

However, the switching capability of Ga_2O_3 vertical Schottky rectifiers has only been demonstrated at low reverse voltages (V_R) .^{23,25,27} There are limited studies on high-voltage switching of Ga_2O_3 Schottky diodes. Furthermore, the practical implementation of high-voltage Ga_2O_3 Schottky rectifier circuits still faces many challenges, such as high-current tolerance and speed constraints from stray board parasitics and the quality of driving signals.

Recently, promising progress in the development and fabrication of $\rm Ga_2O_3$ materials and devices has shown the potential for practical applications. However, due to the limited numbers of prototypes in early development, device model and circuit analysis for realizing $\rm Ga_2O_3$ power electronics is necessary. Some research works²8 investigated the modeling of new $\rm Ga_2O_3$ devices via computer-aided-design (CAD) tools, which helped to speed up device characterization and predicted developed device performance. With accurate parameter extraction and modeling, a circuit-intensive simulator can be used to build power electronic circuits for practical applications and performance improvement.

This paper presents the design flow for device modeling, circuit implementation, $900~V~Ga_2O_3$ device fabrication, and integration of a Ga_2O_3 rectifier. The first section describes how Ga_2O_3 vertical Schottky rectifiers were fabricated on a $20\text{-}\mu\text{m}$ drift layer with a high-voltage switching circuit at 900~V for nanosecond reverse-recovery time. The following section analyzes the design details of the circuit in order to accommodate the high reverse voltage and to enhance the switching speed. The final section presents the measurement results of the proposed circuit design techniques for the Ga_2O_3 vertical Schottky rectifiers.

Fabrication and Characterization of High-Reverse Voltage Ga₂O₃ Schottky Rectifiers

Field-plated, edge-terminated (FPET) vertical Schottky diodes were fabricated on a 20- μm thick Si-doped n-type Ga_2O_3 drift layer grown on a 650- μm thick $\beta\text{-}Ga_2O_3$ substrate using halide vapor phase epitaxy (HVPE). $^{23-26}$ The epi layer growth for Ga2O3 is still developing, and the breakdown voltage of the vertical diode is heavily relating to the number of defects within the drift region. Besides, the breakdown would still occur on the edges of these device contacts. Therefore, a careful fabrication procedure is essential. The $\beta\text{-}Ga_2O_3$ substrate was

¹Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan

²Department of Chemical Engineering, University of Florida, Gainesville, Florida 32611, USA

³Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida 32611, USA

⁴Department of Materials Science and Engineering, University of Florida, Gainesville, Florida 32611, USA

⁵U.S. Naval Research Laboratory, Washington, DC 20375, USA

⁶Tamura Corporation and Novel Crystal Technology, Inc., Saitama 350-1328, Japan

^{*}Electrochemical Society Fellow.

^zE-mail: yudoliao@nctu.edu.tw

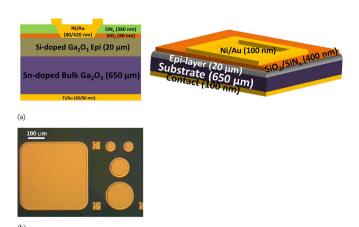


Figure 1. (a) Schematic of field-plated edge-terminated Ga_2O_3 vertical geometry Ni/Au Schottky rectifier structure with a 20- μ m drift layer (b) micrograph of the fabricated Ga_2O_3 diode.

an Sn-doped Ga₂O₃ single crystal wafer with (001) surface orientation grown by the edge-defined film-fed method with a carrier concentration of $3.6\times10^{18}~cm^{-3}$. A back side ohmic contact was formed with electron beam deposited Ti/Au followed by rapid thermal annealing at $550^{\circ}C$ for 30 seconds in nitrogen (N₂). Next, 40 nm of SiO₂ and 360 nm of SiN_x were deposited as dielectric layers. Dielectric contact windows were opened with buffered oxide etchant (BOE). E-beam evaporated Ni/Au (80/420 nm) metallization was used for the Schottky contacts, which overlapped the dielectric windows by 10 μ m. Figure 1 shows a cross-sectional schematic and micrograph of the FPET rectifiers with a dielectric window opening of $400~\mu$ m $\times~400~\mu$ m.

An Agilent 4156C was used to measure the diode DC characteristics up to the equipment's voltage and current limits of 100 V and 100 mA, respectively. Beyond these limits, a Tektronix 370A curve tracer was used to measure the reverse breakdown voltage. A current probe along with a Micsig (DP10013) differential probe were used to characterize the diode switching characteristics. Figure 2a shows the forward-biased diode characteristics that were measured from a 0–1.5 V bias voltage. The extrapolated Schottky barrier height (φ_b) and ideality factors were 1.05 eV and 1.03, respectively, consistent with reported values. 14 The carrier concentration in the drift region was calculated from capacitance-voltage measurements to be 2.01 \times 10^{15} cm⁻³. The diode on-state resistance was 18.2 m Ω -cm², which yields a figure of merit (V_B²/R_{ON}) value of 159 MW-cm⁻². Figure 2b shows the diode reverse characteristics with a reverse breakdown voltage of 1711 V. This high breakdown voltage offers an opportunity for high-voltage power switching applications, such as AC-DC converters and automotive chargers.

Modeling for High-Voltage Ga₂O₃ Vertical Schottky Rectifiers

Based on the current-voltage (I-V) characteristics, essential SPICE parameters of the fabricated Ga_2O_3 diode can be extracted for device modeling with a computer-aided design (CAD) tool. The forward I-V characteristics for these Schottky contacts on a moderately doped drift region were modeled using the thermionic emission model:

$$I = I_{s} \exp\left(\frac{eV}{nkT}\right) \left| 1 - \exp\left(-\frac{eV}{nkT}\right) \right|,$$
 [1]

where e is the electronic charge, k is Boltzmann's constant, n is the ideality factor, T is the temperature, and I_s is the saturation current. The saturation current (I_s) is given by

$$I_s = AA^{**}T^2 \exp(\varphi_b) / kT$$
 [2]

where *A* is the Schottky contact area, A** is the Richardson constant, and φ_b is the Schottky barrier height. The effective Richardson con-

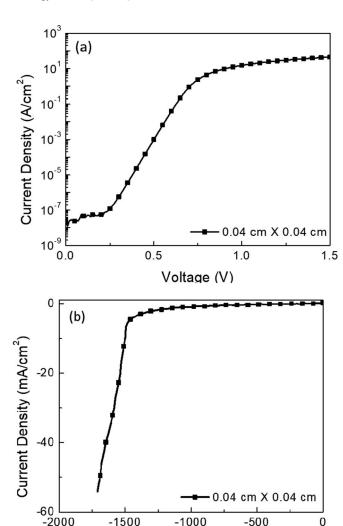


Figure 2. (a) Forward and (b) reverse current density-voltage characteristic for a Ga_2O_3 field-plated rectifier with a breakdown voltage of 1711 V for device size of $0.4 \text{ cm} \times 0.4 \text{ cm}$.

Voltage (V)

stant for Ga₂O₃ has been reported in Ref. 29. In this study, a Richardson constant of 43.35 A.cm⁻².k⁻² was used for calculation of the Schottky barrier heights and ideality factors, and the extrapolation method for these calculations was described by Cheung et al.³⁰

In addition to the static I-V response, dynamic switching characteristics are essential in the power rectifier design. A Ga_2O_3 diode takes a finite time to transit from the reverse bias (off state) to forward bias (on state) state and vice versa. This behavior is crucial for high-power systems since the power loss in the transitions is the significant loss of the switching behavior. A Ga_2O_3 Schottky diode has a minimal current overshoot during the switch from forward-biased conduction to the reverse blocking state because the reverse recovery time only depends on the capacitance, rather than on the minority carrier recombination. However, measuring fast response times at a high reverse voltage remains challenging. Therefore, due to the limitations of the available high-speed and high-voltage measurement instrument, a fast switching circuit was used to verify the Ga_2O_3 rectifier operation in high reverse voltage situations.

Circuit Implementation and Design Considerations for Fast-Switching Ga₂O₃ Diodes

Figure 3a shows the schematic of the rectifier circuit, which consists of an inductor (J.W. Miller 1140–153K-RC, 15 mH), a

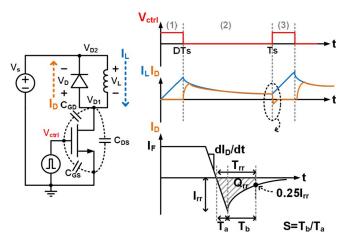


Figure 3. (a) Schematic of switching circuitry (b) voltage and current waveforms of the circuit operations

900 V Ga₂O₃ rectifier, and a power transistor (STMicroelectronics STW9N150, 1.5 kV, 8A n-channel MOSFET) controlled by a pulse signal. Figure 3b shows the operational waveforms of the switching circuit. At startup (region 1), the inductor is charged from the DC power supply to accumulate energy by turning on the power switching transistor. The inductor current can be derived as follows:

$$I_L(t) = \frac{1}{L} \int_0^t V_s d\tau + I_0, \ 0 \le t < DT_s$$
 [3]

where L is the inductance, V_s is the supply voltage, D is the duty cycle of the control signal, and T_s is the period of the control signal. When the power transistor turns off (region 2), the inductor current is discharged through the forward-biased rectifier. The voltage across

the diode then becomes the following:

$$V_{D}(t) = V_{D1} - V_{D2} = (V_{s} - V_{L}) - (V_{s}) = L \frac{dI_{L}(t)}{dt} = L \frac{dI_{D}(t)}{dt},$$

$$DT_{s} \le t < T_{s}$$
[4]

Moreover, the relationship between the inductor current and the diode current can be expressed as follows:

$$I_{L}(t) = I_{D}(t) = I_{s}e^{\frac{eL\frac{dI_{D}(t)}{dt}}{nkT}} \left[1 - e^{\frac{eL\frac{dI_{D}(t)}{dt}}{nkT}} \right], \quad DT_{s} \le t < T_{s} \quad [5]$$

The decayed current at time T_s determines the diode's forward current (I_F). As the power transistor is reactivated (region 3), the Ga_2O_3 device starts transitioning from the on-state to the off-state. The charges in the diode are removed through a reverse current. After the charge carriers in the diode are removed, the diode is reverse biased to provide a high impedance in the discharge path. Eventually, the current reaches zero. The recovered charge Q_{rr} is proportional to the on-state stored charge, which increases with the forward current $(Q_{rr} \propto \sqrt[n]{I_F})$ and can be expressed as stated in Refs. 31,32:

$$Q_{rr} \approx \frac{I_{rr}}{2} * T_{rr} = \frac{I_{rr}}{2} * (T_a + T_b) = \frac{I_{rr}}{2} * T_a * (1 + S)$$
$$= \frac{I_{rr}}{2} * \frac{I_{rr}}{dI_D/dt} * (1 + S)$$
[6]

where T_{rr} is the reverse recovery time, I_{rr} is the peak reverse recovery current, and S is the snappiness factor (also called softness factor), which is determined by the diode construction and the test circuit environment. According to Equation 6, the I_{rr} and T_{rr} can be derived as follows:

$$\begin{cases}
I_{rr} = \sqrt{\frac{2 * Q_{rr} * \frac{dI_D}{dt}}{(1+S)}} = \sqrt{\frac{2 * K_{Qrr} \sqrt[n]{I_F} * \frac{dI_D}{dt}}{(1+S)}} \\
T_{rr} = \frac{2Q_{rr}}{I_{rr}} = \sqrt{\frac{2 * Q_{rr} * (1+S)}{\frac{dI_D}{dt}}} = \sqrt{\frac{2 * K_{Qrr} \sqrt[n]{I_F} * (1+S)}{\frac{dI_D}{dt}}}
\end{cases} [7]$$

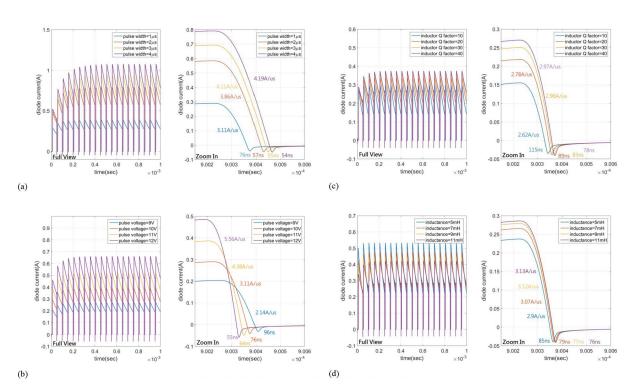


Figure 4. Simulation results of the effects of (a) pulse duration, (b) pulse voltage, (c) Q factor of the inductor, and (d) inductance of the inductor on the T_{IT}.

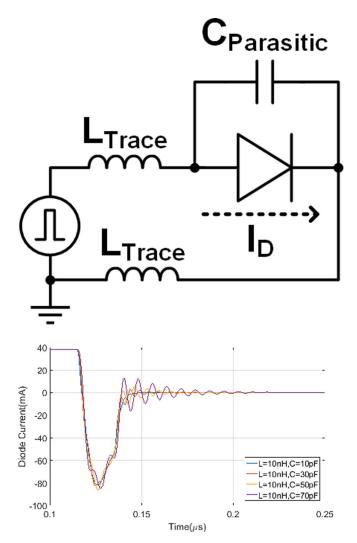
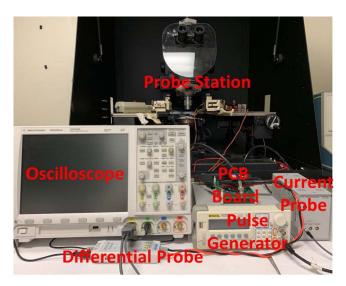


Figure 5. (a) The circuit model of the stray inductance and capacitance from the circuit board and intrinsic diode (b) the simulation results of the damping effects due to the stray parasitics.

This equation shows how the forward current (I_F) and current switching rate (dI_D/dt) affect the reverse recovery behaviors. The I_F and the dI_D/dt can be controlled with the setup of the test board, such as the pulse voltage, pulse duration, inductor values, and quality factor of the inductor. T_{rr} and I_{rr} are simulated using a circuit simulator with the extracted Ga_2O_3 Schottky diode model to verify the switching characteristics. Figure 4 is the simulation of these factors on how to influence the diode reverse recovery behaviors. Regarding the simulation setup, the reverse bias voltage is -900 V, the inductance is 15 mH (Q is about 55), and the transistor is driven by a 10V, 2% duration, 50- μ s period pulse signal.

Figure 4a shows the simulated effects of the duty cycle. The duty cycle is from 2% (1 μ s) to 8% (4 μ s), and the resulting dI_D/dt and T_{rr} are from 3.11 A/ μ s to 4.19 A/ μ s and from 76 ns to 54 ns, respectively. The duty cycle defines the inductor charging time as it relates to the number of accumulated charges stored in the inductor. The longer the on-time of a pulse, the larger the integral forward current. Figure 4b shows the simulation results of the driven voltage from 9 V to 12 V; the values of the dI_D/dt and T_{rr} are from 2.14 A/ μ s to 5.56 A/ μ s and from 96 ns to 55 ns, respectively. The high drive voltage to the transistor results in low on-resistance and also provides a large forward current at a fixed on-time of the pulse signal. The current switching rate also increases with the duration of the pulse, which can improve the reverse recovery time.



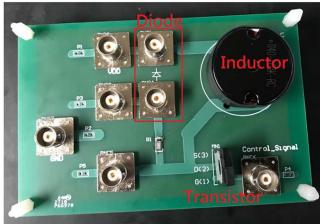


Figure 6. Pictures of the measurement setup and the circuit board.

Furthermore, the off-time of the pulse signal dictates the discharging time, and the amount of forward current before the Ga₂O₃ diode starts switching from the forward state to the reverse-biased state. Thus, the long off-time causes low forward current and current switching rate. In addition to the control signals, the inductor value and quality factor influence the forward current. Figure 4c shows the simulated effects of the inductor Q factor. The Q factor was from 10 to 40, and the resulting dI_D/dt and T_{rr} were from 2.62 A/ μ s to 2.97 A/μs and from 115 ns to 78 ns, respectively. Figure 4d shows the simulation results of the inductance from 5 mH to 11 mH, and the values of the dI_D/dt and T_{rr} were from 2.9 A/ μs to 3.13 A/ μs and from 85 ns to 76 ns, respectively. The energy stored in the inductor was proportional to the inductance and the quality factor when the charging time was constant. Therefore, increasing the quality factor and inductance helped increase the switching rate. However, the switching rate should be limited to prevent high current flow in a short time. Besides, at the reverse recovery of a diode, the oscillation at the abrupt switching of the transistor comes from the resonator circuit of the stray inductance and capacitance along with the diode. Figure 5 shows the simulation results of the influence of stray inductance and capacitance. The oscillation may deteriorate the recovery time of the diode and damping ripples in the switching circuits. Therefore, stray inductance should be minimized by shortening the wire connections.

In summary, T_{rr} can be reduced by increasing the change rate of the forward current (dI_D/dt) or decreasing the absolute forward current (I_F) . Therefore, increasing the dI_D/dt helps to reduce the T_{rr} significantly. In contrast, I_{rr} increases with I_F and dI_D/dt . However,

	J. Yang ²³	J. Yang ²⁵	A. Takatsuka ²⁷	This work
Material	β -Ga ₂ O ₃	β-Ga ₂ O ₃	β -Ga ₂ O ₃	β-Ga ₂ O ₃
Breakdown voltage Switching performance	$T_{rr} = 22 \text{ns} @ \text{from } +2 \text{V to} \\ -2 \text{V}$	760V 1 T _{rr} = 11ns @from +10V to -35V 2 T _{rr} = 64ns I _{rr} = 0.82A @I _F = 1A, V _R = -300V	$T_{rr} = 7.6ns I_{rr} = 0.42A@I_{F}$ $= 1A, V_{R} = -100V$	$T_{rr} = 81 \text{ns } I_{rr} = 38 \text{mA} @ I_{F}$ = 0.3A, $V_{R} = -900 \text{V}$

Table I. Performance summary and comparison with other Ga₂O₃ Schottky diode works.

increasing the change rate of the forward current would increase the I_{rr} and V_{rr} , which may destroy the diode and thus limit its recovery speed.

Experimental Results and Discussion

Figure 6 depicts the measurement setup and the circuit board. The fabricated Ga_2O_3 rectifier was placed on the probe station and wire-connected to the readout PCB for characterization of the reverse recovery dynamics. Figure 7 shows the switching performance of the rectifier. The reverse breakdown voltage of the proposed rectifier was

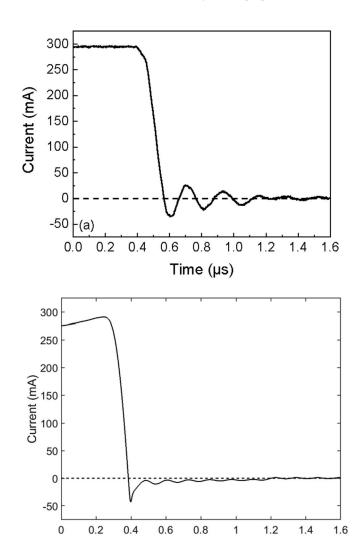


Figure 7. The switching performance of the Ga₂O₃ Schottky diode using the designed circuit board: (a) measured reverse-recovery time versus (b) simulation results.

Time (us)

1711 V. The switching parameters were measured with a forward current of 0.3 A, and the voltage was switched to -900 V. The reverse recovery time was defined as the time required to recover to 25% of the current level of I_{rr} . The fabricated Ga_2O_3 Schottky diode achieved a reverse recovery time of 81 ns, an I_{rr} of 38 mA, and a dI_D/dt of 2.5 $A/\mu s$. During the switching measurements, the pulse used to drive the Si transistor was operated at a period of 50 µs with a duty cycle of 1 μs. The drive voltage of 10 V was applied to the gate of the transistor while the supply voltage was 900 V. Fig. 7b shows the simulation results, which fits the measurement results by adding the cable and trace parasitics with the diode model in the simulation. The extracted stray inductor is about 800nH and 100nF, including the cable and large trace for accommodating large current flowing to the inductor and diode. The design demonstrated a fast recovery response at a very high voltage for the power-switching Ga₂O₃ Schottky diode. Table I shows the performance comparison with the state-of-the-art Ga₂O₃ Schottky diode. The design can achieve a high breakdown voltage and demonstrates a switching voltage up to 900V while T_{rr} is less than 100ns. The careful design to reduce the parasitics on the PCB and cables are required for optimizing T_{rr} of the Ga_2O_3 Schottky diode.

Conclusions

In this paper, a high breakdown voltage vertical Ga_2O_3 Schottky diode was fabricated on a 20- μm thick Si-doped n-type Ga_2O_3 drift layer that demonstrated a 1711 V breakdown voltage and an 81 ns reverse recovery time at a -900 V reverse voltage. A switching circuit using discrete components was implemented in order to achieve a high-voltage switching performance. The design flows, device model and circuit design were analyzed to realize a switching board with the fabricated Ga_2O_3 Schottky diode. Using this Ga_2O_3 Schottky diode design that can operate at a high switchable voltage of up to 900 V brings practical power electronics applications a step closer.

Acknowledgments

The authors would like to thank the Ministry of Science and Technology, Taiwan, for their financial support under the grants MOST 107-2918-I-009-010 and 108-2636-E-009-008. The project at the University of Florida was funded by the Department of Defense, Defense Threat Reduction Agency, HDTRA1-17-1-011 monitored by Jacob Calkins and by NSF DMR 1856662 (Tania Paskova). Research at NRL was partially supported by the Office of Naval Research, under contract N0014-15-1-2392. Research at Novel Crystal Technology is partially supported by ONR Global with grant # N62909-16-1-2217.

ORCID

Fan Ren https://orcid.org/0000-0001-9234-019X
Jenshan Lin https://orcid.org/0000-0002-7439-9259
S. J. Pearton https://orcid.org/0000-0001-6498-1256
Marko J. Tadjer https://orcid.org/0000-0002-2388-2937
Yu-Te Liao https://orcid.org/0000-0002-6868-6729

References

- M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, *Appl. Phys. Lett.*, 100, 013504 (2012).
- Lett, 100, 013504 (2012).

 2. K. Kaneko, T. Nomura, I. Kakeya, and S. Fujita, Appl. Phys. Exp., 2, 075501 (2009).
- G. T. Dang, T. Kawaharamura, M. Furuta, and M. W. Allen, *IEEE Trans Electron Dev*, 62, 3640 (2015).
- H. Zhou, S. Alghmadi, M. Si, G. Qiu, and P. D. Ye, *IEEE Electron Dev Lett*, 37, 1411 (2016).
- M. Higashiwaki, K. Sasaki, T. Kamimura, M. H. Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, *Appl. Phys. Lett.*, 103, 123511 (2013).
- M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, *IEEE Electron Dev Lett.*, 37, 212 (2016).
- K. Sasaki, A. Kuramata, T. Masui, E. G. Víllora, K. Shimamura, and S. Yamakoshi, *Appl. Phys. Exp.*, 5, 035502 (2012).
- K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, *IEEE Electron Dev Lett.*, 34, 493 (2013).
- W. S. Hwang, A. Verma, H. Peelaers, V. Protasenko, S. Rouvimov, H. Xing, A. Seabaugh, W. Haensch, C. Van de Walle, Z. Galazka, M. Albrecht, R. Fornari, and D. Jena, *Appl. Phys. Lett.*, **104**, 203111 (2014).
- K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, *Appl. Phys. Exp.*, 6, 086502 (2013).
- M. Higashiwaki, K. Sasaki, M. H. Wong, T. Kamimura, D. Krishnamurthy, A. Kuramata, T. Masui, S. Yamakoshi, and IEDM Tech, Dig., *Dec.* 28.7.1 (2013).
- V. I. N. S. I. Stepanov, V. E. Bougrov, and A. E. Romanov, Rev. Adv. Mater. Sci, 44, 63 (2016).
- M. Higashiwaki, A. Kuramata, H. Murakami, and Y. Kumagai, J. Phys D-Appl Phys, 50, 23 (2017).
- S. J. Pearton, J. C. Yang, P. H. Cary, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, *Appl. Phys Rev*, 5, (2018).
- H. Xue, Q. He, G. Jian, S. Long, T. Pang, and M. Liu, *Nanoscale Res Lett*, 13, 290, (2018).

- A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch Jr., M. Baldini, A. Fiedler et al., *IEEE Electron Dev Lett*, 37, 902 (2016).
- M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata et al., Semicond. Sci and Technol, 31, 034001 (2016).
- B. J. Baliga, Fundamentals of Power Semiconductor Devices, (Springer Publishing Company, Berlin 2008).
- R. W. Erickson and D. Maksimovic, Fundamentals of power electronics, (Springer Science and Business Media, NY 2007).
- 20. W. E. Forum, (2010, Feb 11th). Forum workshop highlights importance of Smart Grids
- 21. E. Bayoumi, International J. of Industrial Electronics and Drives, 2, 43 (2015).
- https://www.infineon.com/cms/en/product/power/wide-band-gap-semiconductors-sic-gan/silicon-carbide-sic/#
- J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, ECS J. Solid State Sci. Technol, 7, 92 (2017).
- J. Yang, F. Ren, S. J. Pearton, and A. Kuramata, *IEEE Trans Electron Dev*, 65, 2790 (2018).
- J. Yang, F. Ren, Y. Chen, Y. Liao, C. Chang, J. Lin, Marko J. Tadjer, S. J. Pearton, and Akito Kuramata, *IEEE J. Electron Devices Soc*, 7, 57 (2019).
- J. Yang, C. Fares, R. Elhassani, M. Xian, F. Ren, S. J. Pearton, Marko Tadjer, and Akito Kuramata, ECS J. Solid State Sci. Technol. 8, Q3159 (2019).
- A. Takatsuka, K. Sasaki, D. Wakimoto, Q. T. Thieu, Y. Koishikawa, J. Arima et al., in 2018 76th Device Research Conference (DRC), 1 (2018).
- Z. Hu, Hong Zhou, Kui Dang, Yuncong Cai, Zhaoqing Feng, Yangyang Gao, Qian Feng, Jincheng Zhang, and Yue Hao, *IEEE J. Electron Dev Soc*, 6, 815 (2018).
- C. Fares, F. Ren, and S. J. Pearton, ECS J. Solid State Sci. Technol., 8 (2019).
- 30. S. K. Cheung and N. W. Cheung, Appl Phys Lett, 49, 85 (1986).
- O. Al-Naseem, R. W. Erickson, and P. Carlin, Fifteenth Annual IEEE Appl Power Electronics Conference and Exposition, New Orleans, LA, USA, 242 (2000).
- 32. Yueqing Wang, Qingyou Zhang, Jianping Ying, and Chaoqun Sun, IEEE 35th Annual Power Electronics Specialists Conference, Aachen, Germany, 2956 (2004).